

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE - 5.0 Volts
POWER DISSIPATION - 50 WATTS

GENERAL DESCRIPTION

The L05L5V0C6-4C is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).

FEATURES

- Protects up to four high-speed I/O lines & one power line
- Low capacitance: 0.7pF typical (I/O to Gnd)
- Low clamping voltage
- IEC 61000-4-2 (ESD), > ±30KV (air) ; > ±27KV (contact)

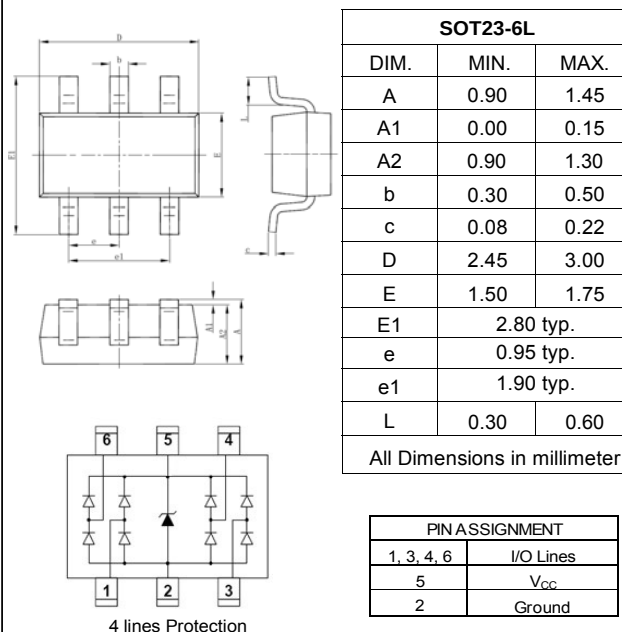
APPLICATION

- USB2.0 Power and Data lines protection
- Digital Visual Interface (DVI)
- Notebook and PC Computers
- Video Graphics Cards
- SIM ports

MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br,Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish)
- Component in accordance to RoHs 2011/65/EU

SOT23-6L



MAXIMUM RATINGS (T_j= 25°C unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Pulse Power (tp = 8/20us)	P _{pk}	50	W
Peak Pulse Current (tp = 8/20us)	I _{pp}	5.5	A
Operating Junction Temperature Range	T _J	-55 to + 125	°C
Storage Temperature Range	T _{stg}	-55 to + 150	°C
Soldering Temperature, t max = 10s	T _L	260	°C

ELECTRICAL CHARACTERISTICS (T_j= 25°C unless otherwise noticed)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse standoff voltage	V _{RWM}	Any pin to ground	---	---	5.0	V
Breakdown voltage	V _{BR}	I _R = 1 mA	6.0	---	9.0	V
Reverse leakage current	I _{RM}	V _{DRM} = 5V	---	---	1	uA
Clamping Voltage	V _C	I _{PP} = 5A, tp = 8/20μs, Any I/O pin to ground	---	8.5	10	V
Junction capacitance	C _J	V _R = 0, f = 1MHz, Between I/O pins	---	0.36	0.5	pF
		V _R = 0V, f = 1MHz, Any I/O pin to ground	---	0.7	1.0	

REV. 0, Sep-2017, KSIR101

FIG.1- 8/20us pulse waveform according to IEC
61000-4-5

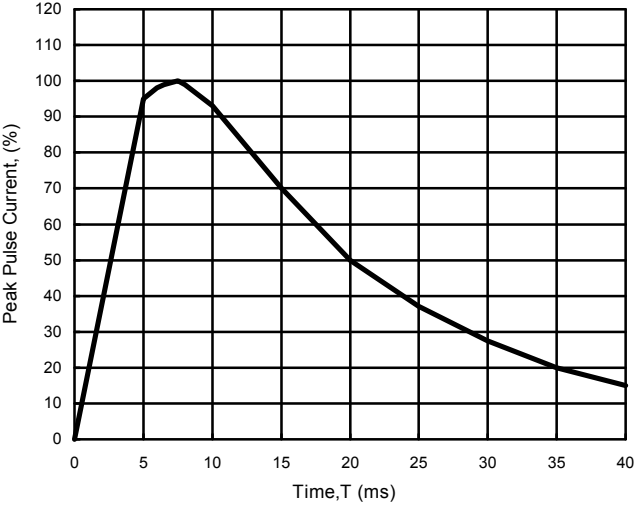


FIG.2- ESD pulse waveform according to IEC
61000-4-2

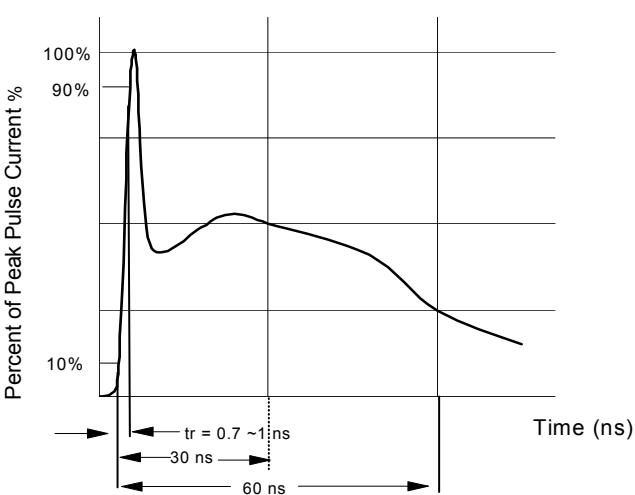


FIG.3- power dissipation versus pulse time

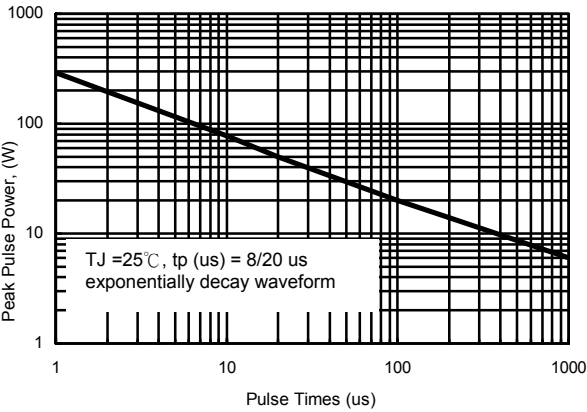


FIG.4- peak pulse power versus T_J

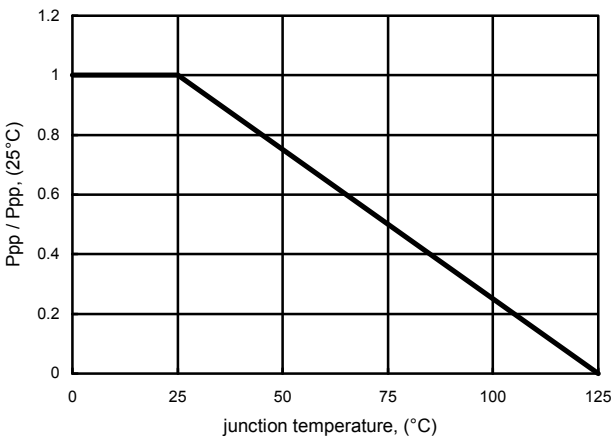


FIG.5- typical junction capacitance

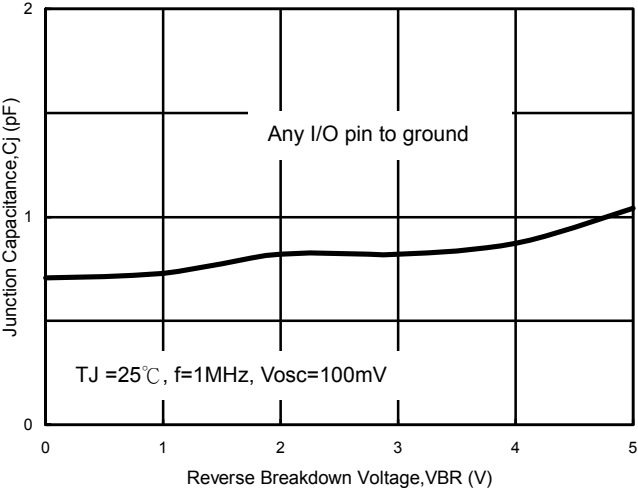
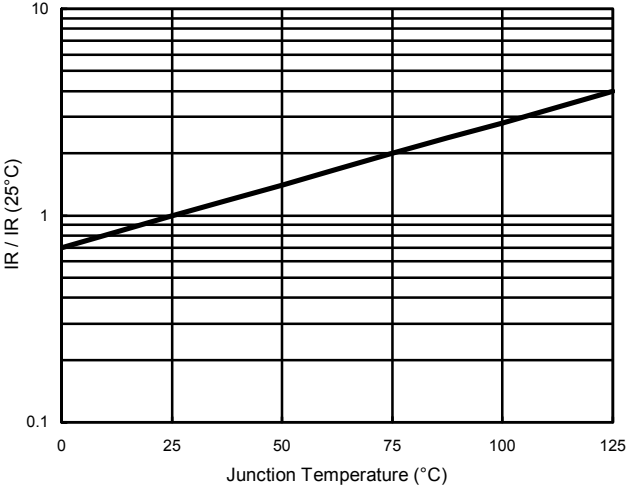


FIG.6- reverse leakage current versus T_J



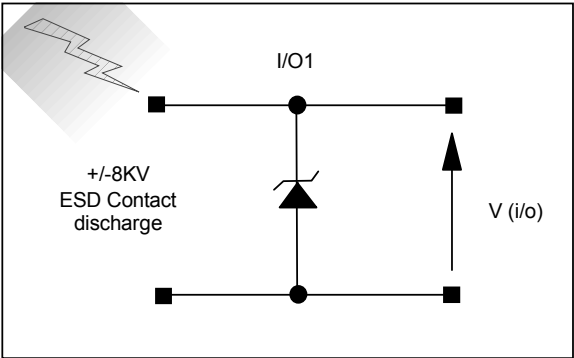


FIG.7- ESD Test Configuration

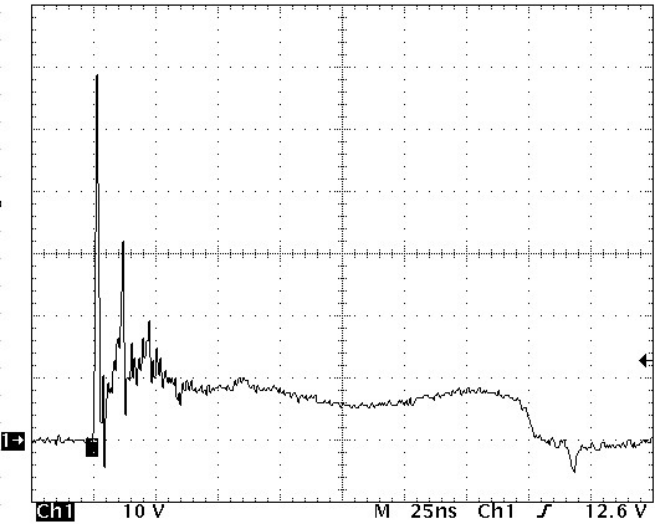


FIG.8- Clamped +8 kV ESD voltage waveform

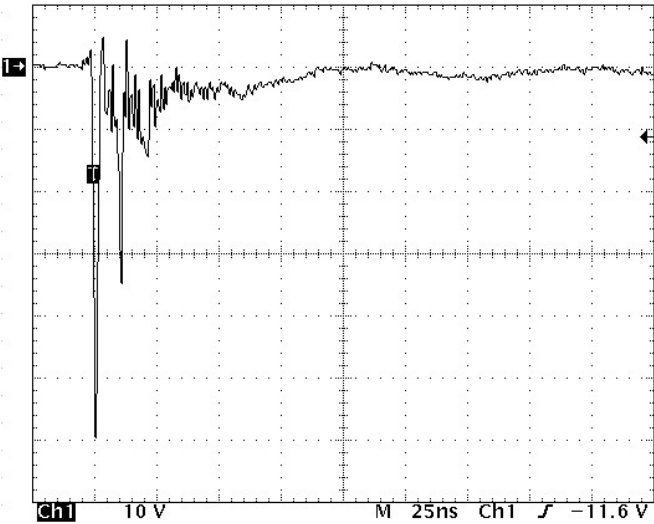
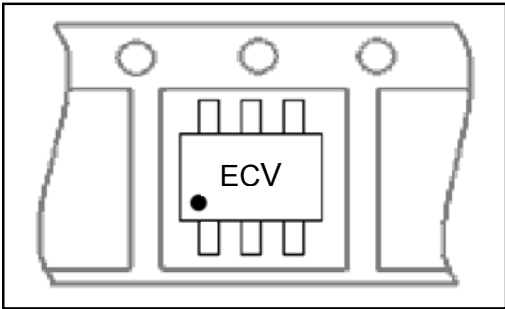


FIG.9- Clamped -8 kV ESD voltage waveform

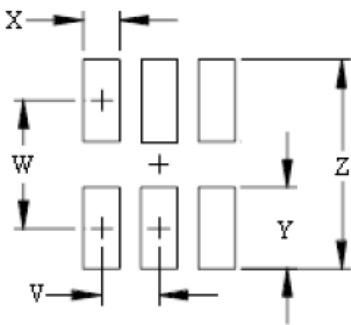
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L05L5V0C6-4C	3000	7	45000	90K/180K

SOT23-6L Soldering Pad Layout



Dim.	Millimeters	Inches
Z	3.60	0.141
X	0.80	0.031
W	2.60	0.102
Y	1.00	0.039
V	0.95	0.037

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